REMARKS

With this Amendment, Claims 8-23 and 25-30 are pending in the present application, Claim 25 is amended and new Claims 29 and 30 are added.

Obviousness under 35 U.S.C. § 103

Claims 8-23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over DiStefano et al. (US 5,821,608) in view of Shiobara et al. (US Patent No. 5,340,851). The Examiner asserted that DiStefano teaches all the limitations of the claims with the exception of a die attach layer (or an adhesive layer) having the properties recited in the rejected claims. The Examiner further asserts that Shiobara teaches a thermosetting resin composition having the recited material properties, and that it would have been obvious to use the material of Shiobara in place of the compliant material (80, 80') of DiStefano. Applicant traverses the rejection and respectfully disagrees with the Examiner's characterization of the prior art.

With regard to Claims 15 and 21, Applicant submits that Shiobara teaches away from the use of a material having a modulus of elasticity within the recited ranges. The examples of thermosetting resin material taught by Shiobara (i.e. examples 1-15 in Table 1) have elastic moduli between about 167 and about 184 ksi (approximate conversions from the values in Table 1, based on 1 kg/mm^2 = 1.42 ksi). Applicant notes that the only example of a material with a modulus of elasticity less than 126 ksi (as recited *inter alia* in Claims 15 and 21) is the "Comparative Example" #4 which is indicated to have a modulus of 87 kg/mm^2 (i.e. about 124 ksi). Applicant notes that Shiobara teaches away from the use of this material by showing high rates of failure in the various tests as compared with the preferred examples 1-15. In fact, Comparative Example #4 has the highest failure rates of all of the comparative examples. Therefore, Applicant submits that it would not have been obvious to use the material of Shiobara in place of the "compliant material" (80, 80') of DiStefano.

With regard to Claim 8, Applicant submits that a person having ordinary skill in the art would not have been motivated to choose such a material for use in the package taught by DiStefano at least because the materials taught by Shiobara have such high elastic moduli that a person having ordinary skill in the art would not have considered the material to be an appropriate material for use in place of the "compliant material 80" in the package of DiStefano. Furthermore, not only is there no affirmative suggestion in the prior art to make

such a substitution, but accepted wisdom as found in the prior art as a whole teaches away from making such a substitution by repeatedly emphasizing the importance of a compliant, low elastic modulus die attach layer. Moreover, such "low modulus" materials also typically have high coefficients of thermal expansion.

Applicant respectfully submits that a person having ordinary skill in the art would not have been motivated to use the thermosetting resin of Shiobara in place of the die attach layer of DiStefano. There is no suggestion in Shiobara that the material described therein would be useful as a die attach layer in an integrated circuit package as recited in Claim 8, nor is there any suggestion in DiStefano to use such a rigid, low CTE material as a die attach layer. Shiobara describes the material therein as being useful as an encapsulant to be molded around a chip, for example, in order to protect the chip from moisture, heat, cracking etc. (see column 15, lines 6-21 and column 16, lines 10-20 and lines 23-34). Although Shiobara suggests use of the resin as an "adhesive," there is no suggestion that the adhesive would be useful in an integrated circuit package.

The Examiner suggested that a person having ordinary skill in the art would have been motivated to make the suggested combination in order to make "the die attach layer easily workable, having improved adhesiveness, improved mechanical strength, hot-water resistance, and minimized water absorption." However, there is no evidence that the material taught by Shiobara would provide improved adhesiveness relative to the other die attach materials used in the prior art. Additionally, the advantages of hot water resistance and minimized water absorption apply to the use of the material of Shiobara as an encapsulant. However, the die attach layer (80) of DiStefano does not encapsulate the package, and thus, the "advantages" of hot water resistance and minimized water absorption are non-sequiteurs in the context of the die attach layer (80) in the package taught by DiStefano, since it is unclear what components would be protected from moisture. With respect to the "advantage" of improved mechanical strength, DiStefano teaches away from seeking a material with increased mechanical strength by repeatedly emphasizing the importance of using a compliant elastomeric die attach material (for example, see Column 1, line 60 through Column 2, line 35).

Moreover, using the material taught by Shiobara in place of the die attach layer of DiStefano would contradict the accepted wisdom in the art of Ball Grid Array (BGA) and similar integrated circuit packages. The accepted wisdom in the art of integrated circuit packages with respect to BGA and similar packages is that a die attach layer (or "compliant layer" or "interposer") should be as flexible as possible (i.e. should have a minimal modulus of elasticity) in order to allow the leads to bend and flex to relieve stresses as the die and the substrate expand and contract at different rates relative to one another (i.e. thermal cycling). As described below, this traditionally requires use of a material with a high CTE.

As described in the prior art of record, Ball Grid Array (BGA), micro Ball Grid Array (μBGA), Tape Ball Grid Array (TBGA) and similar packages often comprise a chip or "die" attached to a substrate with a "compliant layer" configured to relieve stresses due to the thermal mismatch between the die and the substrate. As stated on page 264 in Chapter 16 of John Lau's *Chip Scale Package: Design, Materials, Process, Reliability, and Applications* (cited in the IDS filed 12/5/00):

> The compliant layer of the μBGA is made of silicone elastomer. This is a high-temperature elastomeric material filled with 50 percent of pure silica. As illustrated in Fig. 16.7, the major function of the S-shaped ribbon leads and the compliant layer is to relieve the stresses due to the thermal mismatch between the silicon chip and the substrate. As well as the intrinsic material properties, as indicated in Fig. 16.8, the thickness of the compliant layer may influence the effectiveness of this function as well. In general, a thicker elastomer yields a higher effective CTE but lower package stiffness. Consequently, more stresses due to thermal mismatch may be relieved.

Thus, the prior art of record teaches that the artisan should minimize the stiffness (i.e. the modulus of elasticity) of the compliant layer material, resulting in a higher CTE. Indeed, the above passage suggests that an increased effective CTE caused by an increased compliant layer thickness is acceptable with a corresponding decrease in package stiffness. Thus, not only does the prior art suggest using materials which typically have high CTE's, but the prior art also suggests that the CTE of the die attach layer is an unimportant parameter relative to the elastic modulus of a die attach material. Similar teachings can be found throughout the prior art of record, which repeatedly emphasizes the importance of maximizing the compliance of the connection between the chip and the substrate. For example, see Column

1, line 60 through Column 2, line 35 of DiStefano (U.S. 5,821,608); Column 8, lines 8-14 of U.S. Patent No. 5,347,159 to Khandros et al. which states in part:

> In a fabrication process according to one aspect of the invention, a resilient, compliant layer 64 (FIG. 6) formed from a relatively low elastic modulus material is provided in the lower or downwardly facing space 60 of box element 50. Preferably, this low-modulus material has elastic properties (including modulus of elasticity) comparable to those of soft rubber, about 20 to about 70 Shore A durometer;

Applicant notes that "soft rubber, about 20 to 70 Shore A" typically has a modulus of elasticity between about 0.05 ksi and about 2 ksi depending on the formulation. Also see Column 6, lines 9-33 of U.S. Patent No. 5,148,265 to Khandros et al. which states in part: "The interposer desirably includes a compliant layer of a material having a relatively low elastic modulus, such as an elastomeric material;" Column 11 , lines 49-56 of U.S. Patent No. 5,148,266 to Khandros et al.; and Column 7, lines 8-27 of U.S. Patent No. 6,468,830 to Carson.

In contrast to the teachings of the prior art, embodiments of Applicant's invention include circuit packages with die attach layers made of a more rigid material with a medium modulus of elasticity and a substantially lower coefficient of thermal expansion. In developing the integrated circuit package recited in the claims of the above application, Applicant "proceeded contrary to the accepted wisdom" in the art of circuit packages. "This is 'strong evidence of unobviousness.'" *In re Hedges* 228 USPQ 685, citing *W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 220 USPQ, 303, 312, citing *United States v. Adams*, 148 USPQ 479.

Thus, because each of the rejections of Claims 8-23 relies on the same substitution suggested by the Examiner, Applicant respectfully submits that the devices recited in Claims 8-23 are not rendered obvious by the prior art of record, and Applicant respectfully requests that the rejections be withdrawn.

Claims 25-27 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Khandros et al. (U.S. Patent No. 5,347,159) in view of Shiobara et al. (U.S. Patent No. 5,340,851). The Examiner asserted that it would have been obvious to a person having ordinary skill in the art to replace the compliant layer of Khandros with the resin taught by Shiobara.

Applicant traverses the rejection and respectfully submits that a person having ordinary skill in the art would not have made the suggested substitution because doing so would have required one to go against the accepted wisdom which teaches away from increasing the stiffness of the compliant layer. As noted by the Examiner, Khandros teaches that the compliant material is an elastomer compliant layer with elastic properties comparable to those of soft rubber. Applicant notes that materials such as "soft rubber, about 20 to 70 Shore A durometer" (Col. 8, lines 14-15 of Khandros) typically have very low elastic moduli, often less than one ksi. Thus, by following the teachings of Khandros, a person having ordinary skill in the art would have sought a material having similar "elastic properties." There is no suggestion in the prior art to use a "compliant material" with a substantially increased modulus of elasticity and a substantially decreased coefficient of thermal expansion in place of the "low modulus" materials suggested by Khandros and the other prior art of record. Furthermore, Applicant submits that there is no evidence that the "motivations" suggested by the Examiner would be beneficial in the package of Khandros. Thus, Applicant submits that Claims 25-27 are not rendered obvious by the prior art of record, and respectfully requests that the rejections of these claims be withdrawn.

New Claims

New Claims 29 and 30 further define the invention to include a compliant layer with a modulus of elasticity of between about 50 and about 126 ksi and between about 100 and about 126 ksi respectively. Applicant notes that despite the Examiner's assertions, the thermosetting resin taught by Shiobara does not have a modulus of elasticity within these ranges. Examples 1-15 in Table 1 have elastic moduli of at least 169 ksi (119 kg/mm^2). As discussed above, only the Comparative Example #4 has a modulus less than 126 ksi, and Shiobara teaches away from the use of the material in this comparative example by showing high failure rates in testing of this material. Therefore, Claims 29 and 30 are also believed to be in condition for allowance.

CONCLUSION

Applicant respectfully traverses each of the Examiner's rejections and each of the Examiner's assertions regarding what the prior art shows or teaches. Although amendments have been made, no acquiescence or estoppel is or should be implied thereby. Rather, the

amendments are made only to expedite prosecution of the present application, and without prejudice to presentation or assertion, in the future, of claims on the subject matter affected thereby. Any arguments in support of patentability and based on a portion of a claim should not be taken as founding patentability solely on the portion in question; rather, it is the combination of all of the features or acts recited in a claim which distinguishes it over the prior art. Additionally, any argument made in support of the patentability of a single claim is intended to refer only to the claim which is addressed in the argument, and should not be read as influencing the interpretation of any other claims or claim limitations.

The undersigned has made a good faith effort to respond to all of the rejections and objections in the present application and to place the claims into condition for allowance. Nevertheless, if any issues remain which can be resolved by telephone, the Examiner is respectfully requested to call Applicant's representative at the number indicated below in order to resolve such issues promptly.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 6/29/04

By: _____

Lang J. McHardy
Registration No. 50,591
Agent of Record
Customer No. 20,995
Phone: (805) 547-5584

O:\DOCS\LJM\LJM-3984.DOC
061504

THE μBGA AS A CHIP SIZE PACKAGE

by

Thomas Di Stefano
Tessera, Inc., San Jose, CA 95134

Abstract

The μBGA is a small, thin package with an area array compliant bumps that are attached to substrates by standard SMT reflow and rework processes The μBGA allows connection to substrates of any TCE, because an elastomeric layer in the package decouples the expansion of the chip from that of the substrate. The μBGA package is connected by gold bond ribbons to standard aluminum die pads that can be any where on the die. In its smallest form, the μBGA is a Chip Scale Package, with the compliant bumps arranged under the die. The array of contact bumps can be extended outside the die in a fan in/out configuration. The μBGA is extendible to high I/O, to approximately 1000 I/O for standard perimeter pads, and to higher numbers of I/O for full area array die pads. The μBGA allows the form factor, high I/O, performance, and thermal path of a flip chip in an SMT mountable package.

Introduction

The BGA package has made rapid progress in development and acceptance since its introduction less than 5 years ago. A key factor promoting early acceptance of the BGA was the need for a reduction in form factor for high pin count ICs. By converting from perimeter leads to area array contacts, the physical size of high pin count packages can be reduced significantly. The size advantage of the BGA increases at high I/O because the surface area increases linearly with package I/O rather than with the square of I/O as is the case for the QFP Motorola was among the first to bring the new area array packaging to market as the OMPAC ™. Rapid advances in BGA technology have broadened the scope of applicability of this new SMT technology to thinner packages and higher power.

The μBGA represents the extension of BGA technology to higher I/O, performance, and power in a package that can be nearly as small as the chip[1]. As a Chip Scale Package (CSP), the μBGA approaches the ultimate package size, that of the chip itself[2]. Although small, the μBGA performs all of the functions of a conventional package. It has compliant leads that can be SMT attached to standard PWB substrates[3]. The compliant leads decouple the thermal expansion of the die from that of the substrate without putting undue stress on the solder connections. As with SMT, the μBGA package is reworkable by hot air desoldering of the part. The package is encapsulated and protected from contamination, handling damage, α-particles, and the soldering process. Standards for outline and pin-out can be established. The parts can be socketted, tested and burned-in.

The μBGA provides the performance and form factor advantages of a flip chip in a Chip Scale Packaged format. With its small size and correspondingly small inductance and capacitance, systems built with the μBGA can perform at speeds that are comparable to bare chip MCM-D systems[4]. Because of the short leads, the typical power/ground inductance is on the order of 0.5 nH. A direct back side thermal path is very efficient. Single chip air cooled modules have been demonstrated to power levels of 60 watts on a 12 mm square TI thermal test chip[5]. High performance systems assembled with Chip Scale Packages will provide the form factor, performance and power advantages sought from MCMs without the necessity of handling and testing bare silicon. Since semiconductor

manufacturers can provide fully tested and packaged parts, the customer does not need to solve KGD issues in order to assemble systems with μBGAs.

In order to reduce the size of the μBGA to Chip Scale, several technological challenges had to be overcome. First, the area array of contact bumps needed to be placed over the face of the die. A spacer layer of high temperature elastomer between a flex film with contact bumps and the die surface decouples the thermal expansion of the die from that of the contact bumps. Second, the contact bumps and the pads on the die surface must be interconnected by flexible wiring that accommodates thermal mismatch without fatigue failure. These compliant connections are made by thin gold ribbon leads in a lazy "S" shaped curve that will flex to accommodate relative motion.. And third, bonds must be made to die pads of any type that may be placed anywhere on the face of the die. Techniques were developed to form and bond gold ribbon leads to perimeter pads, center pads, LOC ring pads and full area array pads. Because these short ribbon leads arrayed over the face of the die connect pads to the array of bumps with the shortest lead length possible, the inductance and capacitance of the interconnect is a minimum.

Basic μBGA Structure

The μBGA is an area array of bump contacts on a flexible polyimide film that rests on a thin layer of silicone elastomer. The elastomer supports the film and provides x-y-z compliance. A sectional view of a fan-in μBGA, displayed in schematically Figure 1, shows the array of bumps on a 25 μm thick polyimide film. The flex film is designed with double sided copper on 25 μm of polyimide in order to maintain compliancy of the thin flex film. The elastomer pad is a 150 μm thick film of high temperature silicone elastomer filled with 50% pure silica. In addition to resilient support, the elastomer provides an α barrier necessary to shield the die from potential radioactive impurities in solder used for SMT. The elastomer is attached directly to the face of the die with silicone encapsulant material. Gold ribbon leads connect traces on the flex circuit to aluminum pads on the face of the die.

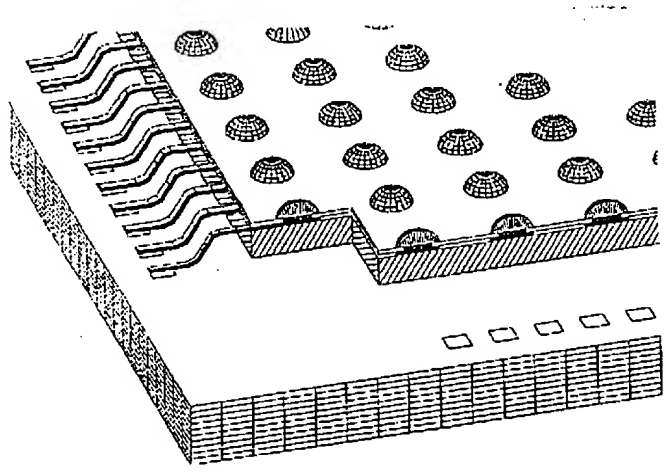

Figure 1 Sectional view of a fan-in μBGA mounted to the face of a die

Each of the ribbon leads has a lazy "S" shape in order to accommodate flexure of the lead during power or temperature cycling. The differential thermal expansion can be significant. For example, during soldering of a 16 mm die to a standard FR-4 circuit panel, the corner bump moves approximately 22 μm in x and y directions with respect to the die. The gold ribbon lead must flex in both the longitudinal and transverse directions. The ribbon is 15-25 μm thick 99.99% gold order to accommodate the flexure without fatigue. The entire structure including the ribbon leads is encapsulated in a low modulus silicone encapsulant in order that there are no points of stress concentration on the leads. A TI X-1379 thermal test chip was used to evaluate thermal, stress, electrical and reliability aspects of the μBGA. The 188 lead chip contains daisy chains, heaters, strain guages, triple tracks and temperature sensing devices. A simple daisy chain chip with the same 188 pin footprint was used for reliability testing. The daisy chain chip shown in Figure 2 is prior

to encapsulation of the bond leads. Gold 25 μm wide aluminum pads on the die. The bump pitch in this case is 0.5 mm. and the bump diameter is 0.3 mm. In the ribbons leads are thermosonically bonded to each of the configuration shown in Figure 2, the wiring is fanned-in over the face of the die to connect the perimeter die pads to the area array of bump contacts. The same type of bond ribbon lead structures are used for center pads, fan-out, fan-in/out and full area array μBGA structures. A range of μBGA types have been fabricated with bump pitch 0.5, 0.635, 1.0 and 1.27 mm bump pitch. The thermal test chip shown in Figure 2 is mounted in a 0.8 mm thick thermal spreader enclosure. The optional enclosure provides additional handling protection for use with automatic insertion equipment. Packaged without the enclosure, the chip is encapsulated with a thin layer of silicone encapsulant over the edge of the die, leaving the a bare back side of the die for thermal contact. In the bare configuration, the encapsulation provides edge protection and a longer path for contamination.

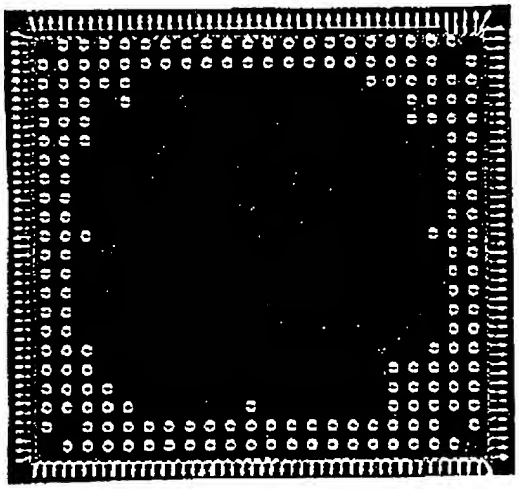

Figure 2 Face of a 188 pin daisy chain test μBGA prior to encapsulation

The μBGA is tested by clamping the compliant contact bumps of the μBGA to a mating socket. In the simplest case for small μBGAs, the socket is a planar array of contact pads fabricated on a flat flex film. A bump compliance of 1-1.25 gF/μm will accommodate some deviation from non-coplanarity in the μBGA. For small μBGAs, a coplanarity within +/- 10 μm will allow test by clamping to planar contacts. Ceramic sockets are generally not sufficiently planar for simple contact without additional compliance In the socket. For large μBGAs, a compliant socket with contact wipe is required for test and burn-in.

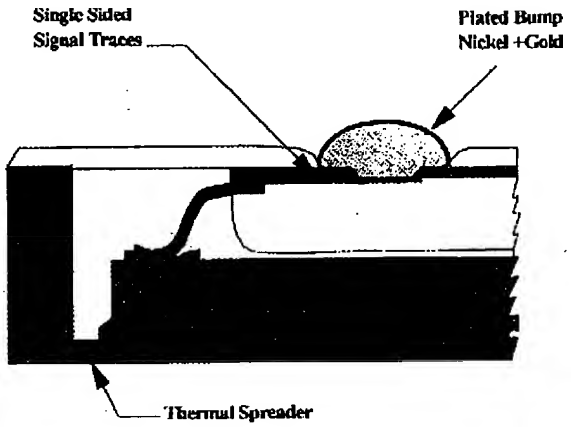

Figure 3 Single metal μBGA with plated post

μBGA Design

The μBGA is designed with one layer of signal and power, and an optional ground layer. The wiring is confined to one or two metal layers so that the wiring layer is flexible and compliant. The simplest design is wired with one metal layer as illustrated in Figure 3. Here the gold ribbon leads connect die pads to the wiring on one side of the flex. Bumps of nickel plated with 0.3 μm of gold form contacts of the bump array. The signal lines are 10 μm copper traces of minimum 25 μm line width and 40 μm spacing. In this case, the bumps extend completely through vias in the flex from the circuit side to the contact side. The bumps are electroplated nickel, plated to a height of 85-90 μm, and coated with a 0.3-0.5 μm flash The single metal μBGA is suitable for applications where controlled impedance and cross talk are not critical. The inductance to the first bump is 0.5-0.7

nH and the typical range for signal line inductance is 0.5-2.1 nH. For high performance μBGA applications, a ground plane is desirable to reduce cross talk, ground bounce, and power/ground inductance. The two metal μBGA in Figure 4 has a 5 μm copper ground plane that is perforated by an array of solder pads.

The ground plane establishes a controlled impedance of 65 Ω for a trace width of 25 μm over the 25 μm polyimide dielectric layer. In addition to controlling impedance, the ground plane provides a degree of shielding of the circuitry on the chip from both the substrate and μBGA signal traces. The 150 μm thick elastomer separates the surface of the die from the signal traces and the associated ground plane. The power and ground leads are kept short and broader than the signal traces in order to minimize inductance. The ground leads are typically wired directly to the ground plane by a blind visa, to keep the lead inductance to 0.3-0.35 nH on the ground plane μBGA.

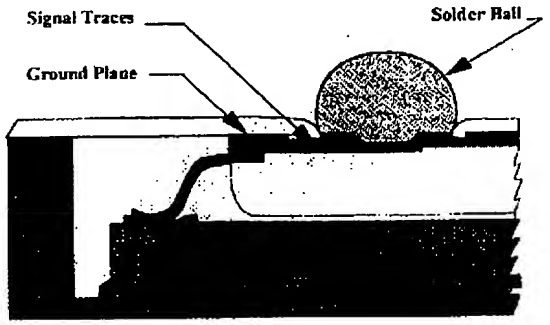

Figure 4 μBGA with solder ball for attachment

Because of the x-y-z compliancy of the μBGA contacts, solid core solder balls can be used for bumps, as shown in Figure 5. Thermally induced shear strain is taken up across the elastomer pad rather than the solder ball. The copper core ball, used on the original IBM flip chip, provides dimensional control over the bump diameter and height that are less dependent upon pad size, solder paste and surface conditions The solid core ball has the interesting feature that it allows a solder fillet to form at the junction of the ball to the pad, for a range of solder volume, pad diameter and ball diameter. The solder fillet acts to relieve stress at the solder-to-pad junction where brittle intermetallics often form. In addition, the solid core ball may be easier to socket since it forms a high aspect ratio bump of controlled diameter. The copper core solder ball is a promising candidate for fine the smaller bumps needed for fine pitch BGAs.

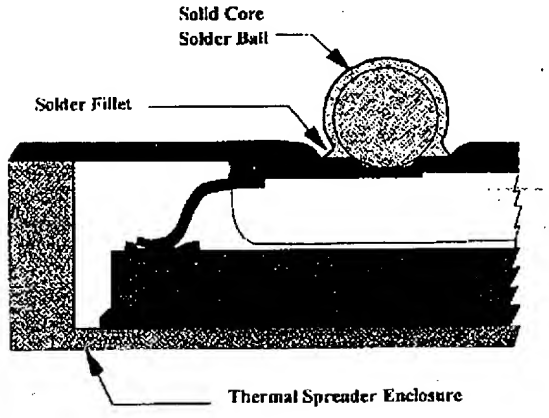

Figure 5 Ground plane μBGA with solid core solder balls

μBGA Roadmap

The μBGA is easily configured as a Chip Scale Package with the bumps arrayed on an elastomeric layer over the face of the die. At the BGA standard bump pitches of 1.0, 1.27 and 1.5 mm, the I/O of the CSP is limited by the number of bumps that will fit under the shadow of the die, as illustrated by the 1.0 mm bump pitch curve in Figure 6. The CSP will accommodate memory chips and other low pin count parts at standard BGA grid pitches

THE μBGA AS A CHIP SIZE PACKAGE

byThomas Di Stefano

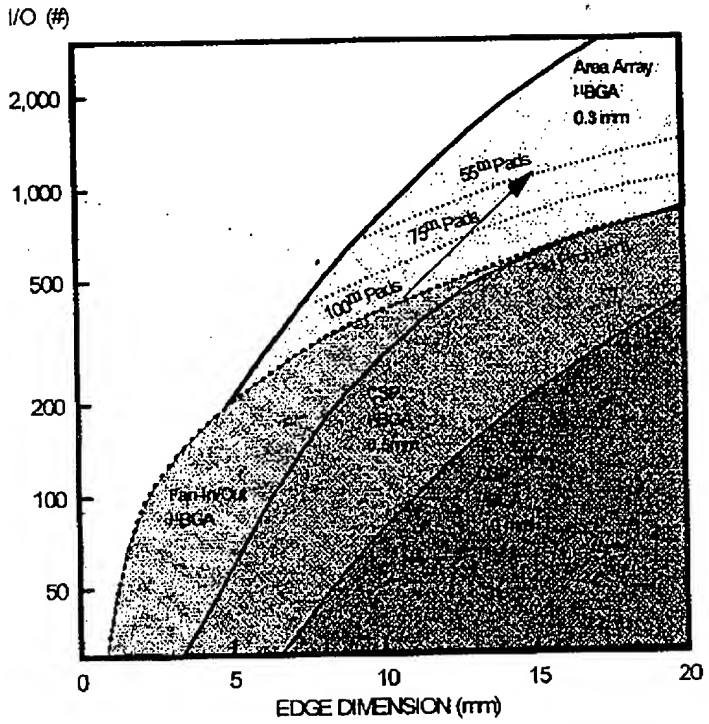

Figure 6 Roadmap of chip I/O for the μBGA for the Chip Scale Package and the fanin/out configuration

For micro-processors and other high pin count ICs, a bump pitch less than 1.0 mm is necessary to wire the I/O on a Chip Scale μBGA. Virtually all of the present day processor chips can be wired in a CSP with a pad pitch of 0.5 mm. Future processor chips are becoming pad limited for I/O approaching 300-500, as indicated by the dotted line in Figure 6. The rising I/O is driving a demand for a smaller pad pitch on perimeter padded ICs. For example, a 1 μm reduction in pitch on a pad limited die translates into a 2% saving in silicon area. By reducing the pad pitch to about 50 μm, all of the μBGA bumps on a 0.5 mm Chip Scale Package can be wired to perimeter pads. Above 1000-1400 I/O, a transition from perimeter pads to area array pads on the die is anticipated.

The μBGA Roadmap extends the I/O capability of the package up to about 4000 by wiring to full array pads on the die. A reduction in μBGA bump pitch to 0.3 mm is necessary above an I/O of 1400. The area array μBGA retains the compliant bump and elastomeric encapsulation used on the standard μBGA package, while allowing bonding over active devices to the array of pads.

In order to wire high I/O BGAs using low cost PWB substrates available today, it is convenient to design for a coarse bump pitch and to limit the number of rows of bumps. Initial applications for the BGA are using 1.27 mm pitch, and 3-4 rows of bumps to make wiring easier. At this coarse pitch, the μBGA must be fanned out or fanned in/out to an array larger than the die itself. In the future, small form factors and cost reduction will drive the development of fine via pitch laminates needed for the high I/O Chip Scale Packages.

The I/O capability of the μBGA has been extended to 55 μm in the laboratory by techniques that allow for better control of the fine pitch bonding process[6]. A reduction of pad pitch to 50 μm enables full wiring capability for a 0.5 mm pitch μBGA Chip Scale Package up to 20 mm die sizes. A roadmap for implementation of

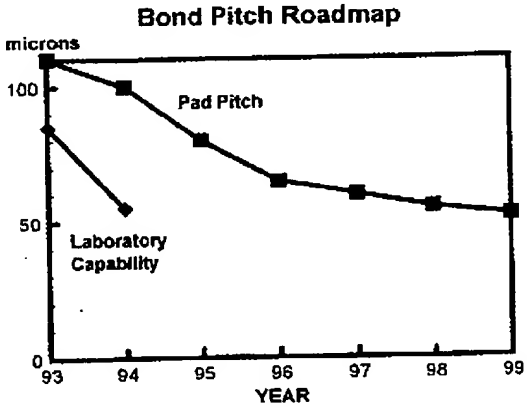

Figure 7 Roadmap for reduction of bond pad pitch on the μBGA

THE μBGA AS A CHIP SIZE PACKAGE

byThomas Di Stefano

Bond Pitch Roadmap

	Pitch P microns	Window W microns	Tool T microns	Tab S microns	Flare F microns	Position B microns	Alignment A microns
1994	100	60	100	50	48	8	25
1995	80	50	85	38	57	6	20
1996	65	45	70	32	48	5	15
1997	60	40	63	30	44	4	15
1998	50	35	55	24	36	3	15
1999	45	35	50	20	31	3	15

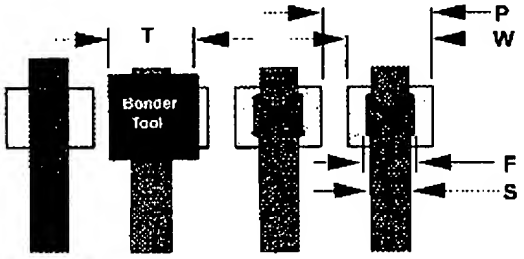

Figure 8 μBGA fine pitch bonding implementation plan

fine pitch bonding, shown in Figure 7, anticipates a 50 μm bond capability on linear rows of pads by 1998.

Implementation of the progression to fine bond pitch is outlined in the chart of Figure 8, showing the critical dimensions. The ribbon leads are bonded to standard aluminum die pads by a single point thermosonic bonding process. The bonder tool is shaped to allow the tool to capture and guide the lead accurately, and to bond the lead to a selected position on the bond pad. During the bonding process, each lead is moved laterally out of the way of the unbonded leads, in a sequential "Zipper Bond" motion that opens up the additional space to allow the bond to be made easily.

Because the lead is repositioned by the tool to align with the bond pad, the initial alignment accuracy "A" is not a critical in determining capability for fine pitch. The critical dimensions limiting the bond pad pitch are the bonder tool dimension, the flare in the bonded lead and the relative accuracy for placement of adjacent leads. Bonds have been made in the laboratory with a 50 μm wide tool "T" and a 25 μm wide ribbon lead. The bond leads are 99.99% gold ribbons 20-25 μm thick. Bonding at a 55 μm pitch has been demonstrated on a linear row of pads. Based on the simple model in Figure 8, the practical limit to the bond pitch is projected to be 45 μm for the near future.

The bonding process can be used to bond ribbon leads to pads anywhere on the face of the die. In the standard process, a bond window is opened over the pad, wherever it lies, and the ribbon is formed and thermosonically bonded to the pad. Leads have been bonded to perimeter pads, center pads, and bumped pads.

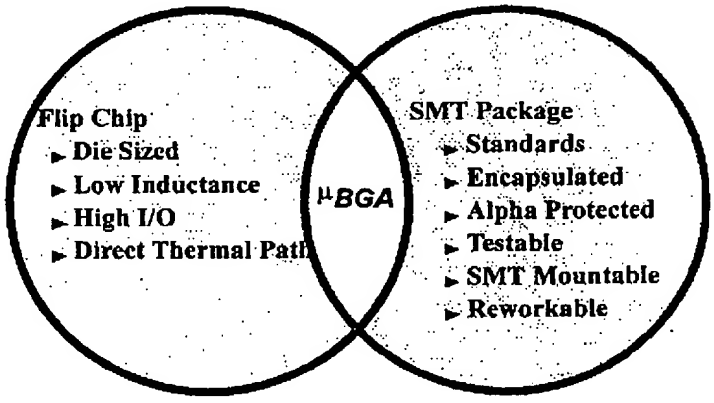

Figure 9 The μBGA brigdes the gap between SMT and flip chip

THE μBGA AS A CHIP SIZE PACKAGE
byThomas Di Stefano

Conclusions

The μBGA allows extension of SMT packaging technology into the foreseeable future. The μBGA provides the performance, I/O, size and cost advantages sought from bare die MCMs The μBGA is a surface mountable package that retains the features commonly assumed to describe a package. The leads are x-y-z compliant, allowing it to attach on any substrate by standard SMT mount and rework techniques. The package is can be tested and burned in and the encapsulated μBGA can be handled with pick and place equipment. Finally, the μBGA can be reduced in size to nearly the size of the chip itself. The fan-in μBGA is a Chip Scale Package, where the compliant package is assembled directly to the face of the die. The μBGA allows extension to finer pad pitch and to chip I/O of 1000-1400 for standard perimeter pads.

References

1. US Patents 5,148,265, 5,148,266 and 5,158,330 assigned to Tessera, Inc.

2. Mohan A. Kirloskar and Thomas Di Stefano, "μBGA: New Chip Size Package," Semicon West, San Francisco, 1994.

3. Mike Loo, Maryjane Krebser, Ali Hassanzadeh and Gill Shook, "Surface Mount Study of Fine Pitch Micro Ball Grid Array," Proceedidngs of the 1994 International Electronics Packaging Conference, September 15-28, 1994, IEPS, pp.555-561.

4. M.Martinez et al., The TCC/MCM: μBGA on a Laminated Substrate," ICMCM Denver, April, 1994.

5. M. Loo and K. Gilleo, "Area Array Chip Carrier SMT Packaging of Known Good Die," Proceedings of the ISHM Conference, pp. 318-323 (1993).

6. Z. Kovac et al. "Fine Pitch Wire Bonding for μBGA Packages," Presented at the 1994 ISHM Conference, Boston, November 15-19, 1994.